CLAIMS

WE CLAIM:

1. A system, comprising:

a table comprising at first timing adjustment signal associated with a rank of a memory component and a second timing adjustment signal associated with the memory component;

a pipeline for imparting a gross timing delay for adjusting the data strobe signal associated with the memory component using a first portion of the first timing adjustment signal; and

a memory cell connected to the pipeline operable for:

receiving at least a second portion of the first timing adjustment signal; and

further adjusting the data strobe signal using the second portion by an amount less than the amount of the first portion.

2. The system of claim 1 further comprising a process for measuring the distribution rate of the data strobe signal and the rate of a data bit arrival time across the memory component.

3. The system of claim 2 further comprising a read data buffer operable for receiving the read data from the memory component and outputting the read data.

4. The system of claim 1, further comprising:

a finite state machine (FSM) operable for determining the rank of at least one memory component from an address associated with the data to be read from the memory component;

5. The system of claim 1, wherein the memory component is a dual data-rate (DDR) memory component.

6. The system of claim 1, wherein the first portion adjusts the data strobe by multiples of a clock pulse, and

wherein the second portion adjusts the position of the data strobe signal by fractions of the clock pulse.

7. The system of claim 1, wherein the second timing adjustment signal is operable for adjusting the data strobe signal.

8. The system of claim 1, wherein the memory cells comprise:

an adjustable pipeline for receiving second portion of the first adjustment signal;

a pulse stretch circuit for generating a gating signal for the data strobe signal;

a logical gate for combining the gating signal with the data strobe signal from the memory component to produce a gated data strobe signal;

a delay clock circuit operable for:

imparting a predefined time delay on the gated data strobe signal; and

adjusting the timing of the data strobe to coincide with the data pulse; and

a logic gate for reading out the data.

9. The system of claim 1, wherein the table is located in a memory controller hub (MCH).

10. The system of claim 1, wherein the table is located within the memory component.

11. A method, comprising:

calculating the rank of the DDR memory component from a command tenure;

extracting at least one timing adjustment signal from a look-up table associated with the calculated rank; and

using the at least one timing adjustment signal to adjust a gating circuit for gating a data strobe signal to account for timing variations for reading data in a memory component.

12. The method of claim 11, further comprising

extracting a second timing adjustment signal from the look-up table associated with the calculated rank and memory component; and

using the second timing adjustment signal to synchronize the gated data strobe signal with the data signal.

13. The method of claim 11, wherein the command tenure comprises a read command and an address associated with the data.

14. The method of claim 11 wherein the at least one timing adjustment signal comprises a first portion and a second portion,

wherein the first portion is used to grossly adjust the gating signal using integer multiples of a clock signal, and

wherein the second portion is used to finely adjust the position of the gating signal using fractions of the clock signal.

15. The method of claim 11, further comprising:

shifting the gated data strobe signal by ¼ of a clock pulse.

16. The method of claim 15, further comprising:

using the shifted data strobe signal to trigger a flip-flop for reading the data.

17. A memory cell; comprising:

an adjustable pipeline operable for:

receiving a fractional portion of a first adjustment signal, the fraction portion having a first value; and

adjusting timing of a gating signal by a length of time equal to the value of the fractional portion of the first adjustment signal;

a pulse stretch circuit for stretching the gating signal in time;

a logical gate for combining the stretched gating signal with a data strobe signal from a targeted memory component to produce a gated data strobe signal;

a delay clock circuit operable for:

imparting a predefined time delay on the gated strobe signal; and

adjusting the timing of the delayed data strobe signal to coincide with the read data pulse; and

a circuit for reading out the data.

18. The memory cell of claim 17, wherein the delay clock circuit is further operable for

receiving a second adjustment signal having a predefined value; and

using the predefined value of the second adjustment signal to adjust the time of the delayed data strobe signal.

19. The memory cell of claim 17, wherein the predefined delay is equal to ¼ of a system clock pulse.

20. The memory cell of claim 19, wherein the value of the fraction portion of the first adjustment signal comprises a fraction portion of the system clock pulse.